In the Claims

CLAIMS

Claims 1-77 (Cancelled).

78. (Currently amended) A method of forming capacitors on a semiconductor device having a substrate, comprising the steps of:

forming a first capacitor electrode supported by said substrate and including roughened polysilicon, said first capacitor electrode having a portion which extends generally vertically relative to said substrate;

forming a dielectric layer over said first capacitor electrode;

forming a second capacitor electrode over ~~a~~ one portion of said dielectric layer such that ~~an other~~ another portion of said dielectric layer is exposed relative to said second capacitor electrode; and

forming a dielectric barrier over said exposed portion of said dielectric layer.

79. (Previously presented) The method of claim 78, wherein said exposed portion of said dielectric layer comprises an uppermost portion of said dielectric layer.

80. (Currently amended) The method of claim 78, wherein the dielectric barrier extends at least in part above said first capacitor electrode, said dielectric layer and said second capacitor electrode.

81. (Previously presented) The method of claim 78, further comprising the steps of:

forming an opening in said dielectric barrier: and

forming a conductive element extending into said opening to form an electrically conductive contact to said second capacitor electrode.

82. (Previously presented) The method of claim 78, wherein said exposed portion of said dielectric layer comprises an uppermost portion of said capacitors.

83. (Previously presented) The method of claim 78, wherein said exposed portion of said dielectric layer is spaced apart from said first capacitor electrode.

84. (Previously presented) The method of claim 78, wherein said exposed portion of said dielectric layer is spaced apart from and directly over said first capacitor electrode.

85. (Previously presented) The method of claim 78, further comprising insulative material elevationally below and contacting said exposed portion of said dielectric layer.

86. (Currently amended) The method of claim 78, wherein said exposed portion of said dielectric layer is spaced apart from the first capacitor electrode, and wherein ~~said dielectric layer comprises other portions contacting~~ the one portion of said dielectric layer contacts said first capacitor electrode.

87. (Previously presented) The method of claim 78, wherein at least one of said first and second capacitor electrodes extends substantially vertically relative said substrate.

88. (Currently amended) A method of manufacturing a semiconductor device having capacitors thereon, comprising the steps of:

forming first and second capacitor electrodes supported by a semiconductor substrate, each said capacitor electrode having a portion extending vertically relative to said substrate, said first and second capacitor electrodes being electrically isolated from each other;

forming a first dielectric layer extending over at least a portion of both of said first and second capacitor electrodes, said first dielectric layer extending over at least an uppermost portion of each of said first and second capacitor electrodes;

forming a conductive layer extending over said first dielectric layer and above said first and second capacitor electrodes;

selectively removing selected portions of said conductive layer to expose a first portion of said first dielectric layer relatively proximate said substrate, and to expose second and third portions of said first dielectric layer relatively remote from said substrate, and to electrically isolate sections of said conductive layer to form a third capacitor electrode in contact with a portion of said first dielectric layer proximate said first capacitor electrode, and a fourth capacitor electrode in contact with a portion of said first dielectric layer proximate said second capacitor electrode, said third and fourth capacitor electrodes forming cell electrodes of respective first and second capacitors and being electrically isolated from one another; and

forming a second dielectric layer over said exposed portions of said first dielectric layer and over said third and fourth capacitor electrodes.

89. (Previously presented) The method of claim 88, further comprising the step of forming a conductive line extending through said second dielectric layer and contacting said third and fourth capacitor electrodes to establish electrical communication between said capacitor electrodes.

90. (Previously presented) The method of claim 88, wherein said second dielectric layer is in contact with said first dielectric layer and with said third and fourth capacitor electrodes.

91. (Previously presented) The method of claim 88, wherein said second and third portions of said first dielectric layer comprise an uppermost portion of said capacitors.

92. (Previously presented) The method of claim 88, wherein said second and third portions of said first dielectric layer are spaced apart from respective said first and second capacitor electrodes.

93. (Currently amended) A method of forming capacitors, comprising:

forming first and second capacitor electrodes supported by a substrate, the first and second capacitor electrodes comprising respective uppermost surfaces relative the substrate; ~~and~~

forming a dielectric layer disposed between the first and second capacitor electrodes, the dielectric layer comprising an uppermost surface relative the substrate, the uppermost surface of the dielectric layer being ~~elevational~~ elevationally above one of the uppermost surfaces of the first and second capacitor electrodes and being coextensive with the other of the uppermost surfaces of the first and second capacitor electrodes; and

wherein the first and second capacitor electrodes and the dielectric layer form a single capacitor, and wherein the first and second capacitor electrodes are operatively isolated from adjacent capacitors.

94. (Previously presented) The method of claim 93, wherein at least one of the first and second capacitor electrodes is oriented substantially vertically relative the substrate.

95. (Currently amended) The method of claim 93, further comprising insulative material elevationally directly below and supporting ~~contacting~~ the uppermost surface of the dielectric layer.

96. (Previously presented) The method of claim 93, further comprising insulative material elevationally directly above and contacting the uppermost surface of the dielectric layer.

97. (Currently amended) The method of claim 93, further comprising a first insulative layer elevationally below and supporting ~~contacting~~ the uppermost surface of the dielectric layer, and further comprising a second insulative layer elevationally above and contacting the uppermost surface of the dielectric layer.

98. (New) The method of claim 78, wherein the roughened polysilicon comprises hemispherical grain polysilicon.

99. (New) The method of claim 78, wherein the roughened polysilicon comprises cylindrical grain polysilicon.

100. (New) The method of claim 88, further comprising forming a bit line elevationally below the first, second, third and fourth capacitor electrodes and elevationally below the first and second dielectric layers.